IN THE CLAIMS

Please amend the claims as follows:

Claims 1-20 (canceled)

Claim 21 (new): A semiconductor integrated circuit comprising:

an FET having a gate terminal configured to input a controlled signal with a predetermined frequency and a drain terminal configured to output a signal corresponding to said controlled signal;

an inductor element provided between a source terminal of said FET and a ground terminal, said inductor element having an inductance value selected in accordance with the predetermined frequency of said controlled signal and forming a series resonance circuit with a reactance component of a gate-to-source impedance when a drain voltage of said FET is lower than a source voltage thereof; and

a second capacitor element provided between the gate terminal and the source terminal of said FET,

wherein when a drain voltage of said FET is lower than a source voltage thereof, a series resonance circuit is formed of the reactance component of the gate-to-source impedance and said inductor element, and the inductance value of said inductor element is set in accordance with said predetermined frequency of said controlled signal, and

a capacitance value of said second capacitor element is set so that a parasitic resistance component of said FET apparently decreases when the drain voltage of said FET is lower than the source voltage thereof.

Claim 22 (new): The semiconductor integrated circuit according to claim 21, further comprises a control signal input circuit, connected to the drain terminal of said FET, configured to switch and controlling the magnitude relationship between the drain voltage and the source voltage of said FET.

Claim 23 (new): The semiconductor integrated circuit according to claim 22, wherein said control signal input circuit sets a drain-to-source voltage so that $Cgd / (Cgd + Cgs) \cdot Rds / (Rds + RL)$, which is a function of the gate-to-drain capacity Cgd, gate-to-source capacity Cgs, drain-to-source resistance Rds and load resistance RL of said FET, is minimum when the drain voltage of said FET is lower than the source voltage thereof.

Claim 24 (new): A semiconductor integrated circuit comprising:

an FET having a gate terminal configured to input a controlled signal with a predetermined frequency and a drain terminal configured to output a signal corresponding to said controlled signal;

an inductor element provided between a source terminal of said FET and a ground terminal, said inductor element having an inductance value selected in accordance with the predetermined frequency of said controlled signal and forming a series resonance circuit with a reactance component of a gate-to-source impedance when a drain voltage of said FET is lower than a source voltage thereof; and

a second capacitor element provided between the drain terminal and the source terminal of said FET,

wherein when a drain voltage of said FET is lower than a source voltage thereof, a series resonance circuit is formed of the reactance component of the gate-to-source

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impedance and said inductor element, and the inductance value of said inductor element is set

in accordance with said predetermined frequency of said controlled signal, and

a capacitance value of said second capacitor element is set so that a parasitic

resistance component of said FET apparently decreases when the drain voltage of said FET is

lower than the source voltage thereof.

Claim 25 (new): The semiconductor integrated circuit according to claim 24, further

comprises a control signal input circuit, connected to the drain terminal of said FET,

configured to switch and controlling the magnitude relationship between the drain voltage

and the source voltage of said FET.

Claim 26 (new): The semiconductor integrated circuit according to claim 25, wherein

said control signal input circuit sets a drain-to-source voltage so that C_{gd} / (C_{gd} + C_{gs}) · R_{ds}

/ (R_{ds} + RL), which is a function of the gate-to-drain capacity C_{gd}, gate-to-source capacity

C_{gs}, drain-to-source resistance R_{ds} and load resistance RL of said FET, is minimum when

the drain voltage of said FET is lower than the source voltage thereof.

Claim 27 (new): A semiconductor integrated circuit comprising:

an FET having a gate terminal configured to input a controlled signal with a

predetermined frequency and a drain terminal configured to output a signal corresponding to

said controlled signal;

an inductor element provided between a source terminal of said FET and a ground

terminal, said inductor element having an inductance value selected in accordance with the

predetermined frequency of said controlled signal and forming a series resonance circuit with

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a reactance component of a gate-to-source impedance when a drain voltage of said FET is lower than a source voltage thereof; and

a control signal input circuit, connected to the drain terminal of said FET, configured to switch and controlling the magnitude relationship between the drain voltage and the source voltage of said FET,

wherein said control signal input circuit sets a drain-to-source voltage so that $Cgd / (Cgd + Cgs) \cdot Rds / (Rds + RL)$, which is a function of the gate-to-drain capacity Cgd, gate-to-source capacity Cgs, drain-to-source resistance Rds and load resistance RL of said FET, is minimum when the drain voltage of said FET is lower than the source voltage thereof.

Claim 28 (new): A semiconductor integrated circuit comprising:

an FET having a gate terminal configured to input a controlled signal with a predetermined frequency and a drain terminal configured to output a signal corresponding to said controlled signal;

an inductor element provided between a source terminal of said FET and a ground terminal, said inductor element having an inductance value selected in accordance with the predetermined frequency of said controlled signal and forming a series resonance circuit with a reactance component of a gate-to-source impedance when a drain voltage of said FET is lower than a source voltage thereof; and

a bias supply circuit configured to supply a dc bias voltage to at least one of the gate terminal, drain terminal and source terminal of said FET.

Claim 29 (new): A semiconductor integrated circuit comprising:

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an FET having a gate terminal configured to input a controlled signal with a

predetermined frequency and a drain terminal configured to output a signal corresponding to

said controlled signal;

an inductor element and a first capacitor element which are connected to each other in

series between a source terminal of said FET and a ground terminal, said inductor element

having an inductance value selected in accordance with the predetermined frequency of said

controlled signal and forming a series resonance circuit with a reactance component of a gate-

to-source impedance when a drain voltage of said FET is lower than a source voltage thereof;

and

a second capacitor element provided between the gate terminal and the source

terminal of said FET,

wherein when a drain voltage of said FET is lower than a source voltage thereof, a

series resonance circuit is formed of the reactance component of the gate-to-source

impedance and said inductor element, and the inductance value of said inductor element is set

in accordance with said predetermined frequency of said controlled signal, and

a capacitance value of said second capacitor element is set so that a parasitic

resistance component of said FET apparently decreases when the drain voltage of said FET is

lower than the source voltage thereof.

Claim 30 (new): The semiconductor integrated circuit according to claim 29, further

comprises a control signal input circuit, connected to the drain terminal of said FET,

configured to switch and controlling the magnitude relationship between the drain voltage

and the source voltage of said FET.

Claim 31 (new): The semiconductor integrated circuit according to claim 30, wherein said control signal input circuit sets a drain-to-source voltage so that $Cgd / (Cgd + Cgs) \cdot Rds / (Rds + RL)$, which is a function of the gate-to-drain capacity Cgd, gate-to-source capacity Cgs, drain-to-source resistance Rds and load resistance RL of said FET, is minimum when the drain voltage of said FET is lower than the source voltage thereof.

Claim 32 (new): A semiconductor integrated circuit comprising:

an FET having a gate terminal configured to input a controlled signal with a predetermined frequency and a drain terminal configured to output a signal corresponding to said controlled signal;

an inductor element and a first capacitor element which are connected to each other in series between a source terminal of said FET and a ground terminal, said inductor element having an inductance value selected in accordance with the predetermined frequency of said controlled signal and forming a series resonance circuit with a reactance component of a gate-to-source impedance when a drain voltage of said FET is lower than a source voltage thereof; and

a second capacitor element provided between the drain terminal and the source terminal of said FET,

wherein when a drain voltage of said FET is lower than a source voltage thereof, a series resonance circuit is formed of the reactance component of the gate-to-source impedance and said inductor element, and the inductance value of said inductor element is set in accordance with said predetermined frequency of said controlled signal, and

a capacitance value of said second capacitor element is set so that a parasitic resistance component of said FET apparently decreases when the drain voltage of said FET is lower than the source voltage thereof.

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Claim 33 (new): The semiconductor integrated circuit according to claim 32, further comprises a control signal input circuit, connected to the drain terminal of said FET, configured to switch and controlling the magnitude relationship between the drain voltage and the source voltage of said FET.

Claim 34 (new): The semiconductor integrated circuit according to claim 33, wherein said control signal input circuit sets a drain-to-source voltage so that $Cgd / (Cgd + Cgs) \cdot Rds / (Rds + RL)$, which is a function of the gate-to-drain capacity Cgd, gate-to-source capacity Cgs, drain-to-source resistance Rds and load resistance RL of said FET, is minimum when the drain voltage of said FET is lower than the source voltage thereof.

Claim 35 (new): A semiconductor integrated circuit comprising:

an FET having a gate terminal configured to input a controlled signal with a predetermined frequency and a drain terminal configured to output a signal corresponding to said controlled signal;

an inductor element and a first capacitor element which are connected to each other in series between a source terminal of said FET and a ground terminal, said inductor element having an inductance value selected in accordance with the predetermined frequency of said controlled signal and forming a series resonance circuit with a reactance component of a gate-to-source impedance when a drain voltage of said FET is lower than a source voltage thereof; and

a control signal input circuit, connected to the drain terminal of said FET, configured to switch and control the magnitude relationship between the drain voltage and the source voltage of said FET,

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wherein when a drain voltage of said FET is lower than a source voltage thereof, a series resonance circuit is formed of the reactance component of the gate-to-source impedance and said inductor element, and the inductance value of said inductor element is set in accordance with said predetermined frequency of said controlled signal, and

said control signal input circuit sets a drain-to-source voltage so that Cgd / (Cgd + Cgs) · Rds / (Rds + RL), which is a function of the gate-to-drain capacity Cgd, gate-to-source capacity Cgs, drain-to-source resistance Rds and load resistance RL of said FET, is minimum when the drain voltage of said FET is lower than the source voltage thereof.